Gated Silicon Field Emitter Array Characterization

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Abstract: *Arrays of silicon (Si) field emitter tips are being studied for use as electron source for vacuum nano-transistors. These arrays are analyzed using the CST particle tracking solver and via experiment. Simulations are used to study the potential transfer characteristics and performance for use as transistors for the vertical emitter structures. An experimental system has been developed to test the arrays under high temperature (400^O C) and for various gases to study the noise characteristics and the effects of adsorption and desorption on performance.*

Keywords: Field emitter array; field emission simulation; transfer characteristics experiment

Introduction

To exploit new architectures for transistors that combine the positive attributes of semiconductor electronic devices (i.e. high gain, low noise) with the positive attributes of vacuum electronic devices (i.e. high power and high efficiency), cold cathodes that operate with high current and high current density at low operating voltages are being studied. Current state-of-the-art approaches such as those reported in [1, 2] do not simultaneously exhibit all these attributes, resulting in significant compromises in the projected system performance. The primary objective of this work is to characterize the Si vacuum nano-electronic cold cathodes [1] for use as vacuum nano-transistors. The arrays studied here consist of silicon emitter tips surrounded by a self-aligned gate, and these arrays have been studied by simulation and experiment.

Simulation and Experiment

Simulation was carried out using commercially available CST 2019 particle tracking solver [3] using a simple model as shown in Fig. 1. A gate voltage sweep from 0 to 15V was carried out at a fixed collector voltage of 20V. A collector sweep was also carried out from 0 to 20V at a fixed gate voltage of 15V. A schematic of simulation model is shown in Fig. 1(a) where Fig. 1(b) shows the simulated electric field on the tip The calculated field enhancement factor is ~ 2.3×10^2. Key requirements of a transistor are low operating voltage, low emitter to gate current, and limited effects of the collector on the operating current.

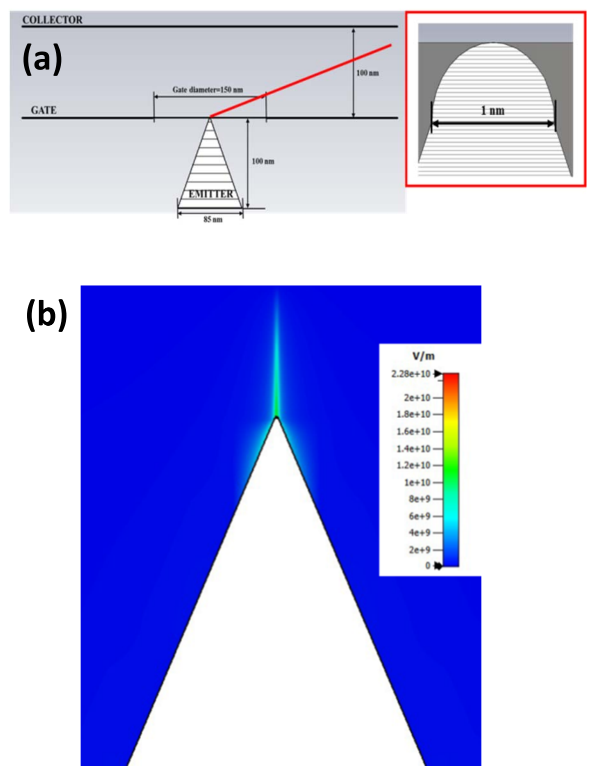

Figure 1. (a) Schematic of simulation model (b) Large scale field enhancement on tip.

Ideal figures of merit could be defined as a low emitter to gate current (<0.01) over the operating range and a low variation in collector current over the collector voltage swing (<0.01). These effects are being studied

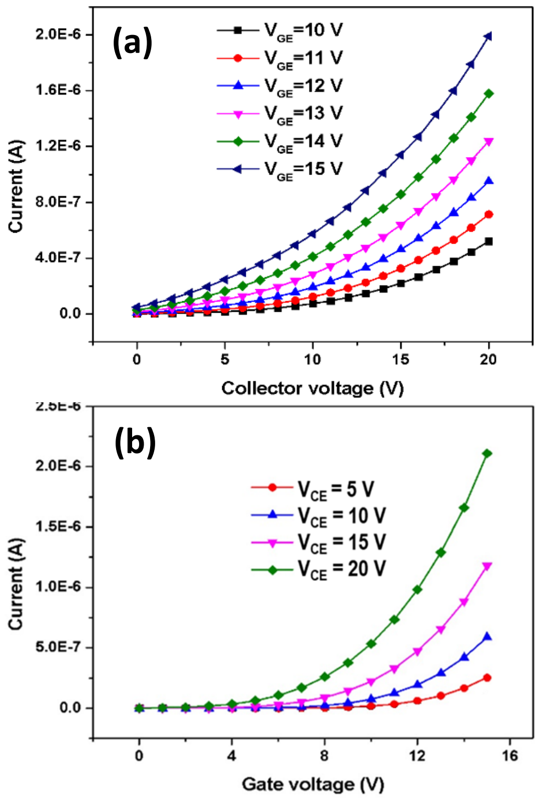

Figure 2. Simulated (a) Output and (b) Transfer characteristics.

via simulation. Shown in Fig. 2 are the variation in collector current vs. collector voltage (Fig. 2(a)) for various gate voltages and the variation in collector current vs. gate voltage (Fig. 2(b)) for various collector voltages.

Initial experimental results (Fig. 3(a)) carried out on emitter arrays [1] using our new test system shows that field emission performance is repeatable and consistent in the setup for a fixed collector voltage of 100V. This setup is also capable of testing at high temperature (400° C) and over a range of pressures (10^{-8} to 760 torr). Various gases can be used including Ar, He, and N. The system uses a source measurement unit (SMU) to drive the arrays in DC operation while measuring collector and gate currents. An arc detection circuit is being developed to monitor the arrays during operation to look for gate to emitter arcs. The emission current can also be studied for noise to look at the effects of adsorption/desorption based on temperature.

A schematic of the test jig is shown in Fig. 3(b). A Molybdenum chuck has been fabricated to use as the heating block to prevent outgassing at high vacuum. A Low Temperature Co-fired Ceramic (LTCC) electrically insulates the silicon arrays from the metal chuck so that the emitter tip current can be measured.

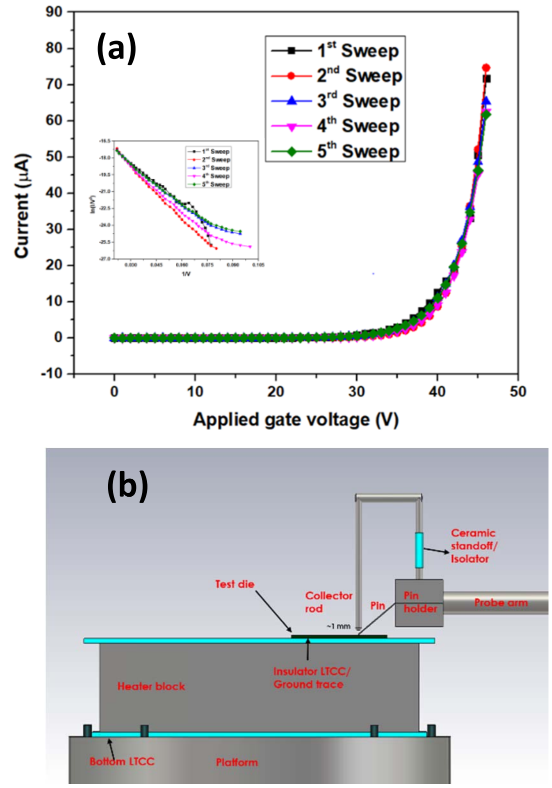

Figure 3. (a) Experimental transfer characteristics (inset: F-N plot), (b) Schematic of test setup showing collector and heater chuck.

Summary

We have analyzed gated silicon field emitter arrays for use as vacuum transistors by using simulation and by developing a test system to allow a range of measurements for a variety of conditions. Preliminary experimental results indicated that we can measure these devices consistently, and new experiments will characterize the device performance versus temperature and background gas pressure.

Acknowledgement

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References

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[3] CST Studio Suite 2019.